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REMARKS

In the last Office Action, claims 1, 2, 4, 11, 15, 16, 43 and 54 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,554,873 to Erdeljac et al. in view of U.S. Patent No. 4,559,694 to Yoh et al. The Examiner stated that Erdeljac et al. disclose a complementary MOS semiconductor device in Fig. 11 having an N-channel MOS transistor 44, a P-channel MOS transistor 50 and a resistor. The Examiner acknowledged that Erdeljac et al. do not disclose that the N-channel MOS transistor has a P-type gate electrode 24 and the P-channel MOS transistor has a P-type gate electrode 24, but pointed out that Figs. 59 and 60 of Yoh et al. disclose a complementary MOS semiconductor device having an N-channel MOS transistor Q4 with a P-type gate electrode and a P-channel MOS transistor Q1 with a P-type gate electrode. In view of this disclosure, the Examiner has taken the position that it would have been obvious to form the gate electrodes 24 of the P-channel MOS transistor 50 and the N-channel MOS transistor 44 of Erdeljac et al. of P-type polycrystalline silicon instead of N-type in order to obtain transistors having low threshold voltages that can operate at low voltage and consume low power.

By the present response, the specification has been amended in minor respects to correct informalities. Claims 1, 2, 4, 11, 15, 16, 43 and 54 have been amended in formal respects to improve the wording and place them in better conformance with U.S. practice. Claim 1 has been further amended to more particularly point out and distinctly claim the novel aspects of the present invention.

Applicants respectfully submit that amended claims 1, 2, 4, 11, 15, 16, 43 and 54 patentably distinguish over the prior art of record and that the non-amended dependent claims should be allowed since they depend upon generic claim 1.

The present invention relates to a power management semiconductor device such as a voltage detector, a voltage regulator, or an analog device such as an operational amplifier or a comparator, and to a method of manufacturing such semiconductor device so as to have a low voltage operation, low power consumption and a high driving capacity.

The conventional CMOS semiconductor device of Fig. 89 has an NMOS transistor 213 with a gate electrode formed of N+ type polysilicon on a P-type semiconductor substrate and a PMOS transistor 212 with a gate electrode formed of N+ type polysilicon in an N-well region of the P-type substrate. A resistor 215 used in a voltage dividing circuit for dividing a voltage or used for setting a time constant is formed on a

field insulating film provided on the substrate. The resistor is formed of the same polysilicon layer used to form the N-type gate electrode.

A typical enhancement type NMOS (or E-type NMOS) has a threshold voltage of approximately 0.7 V and has a gate electrode formed of N+ polycrystalline silicon. Such a transistor is a surface channel device with a channel region formed on a surface of the substrate based on a well-known relationship between the gate electrode and the semiconductor substrate. On the other hand, an enhancement type PMOS (or E-type PMOS) with a typical threshold voltage of about -0.7 V is a buried channel device having a channel buried somewhat beneath the surface of the substrate in accordance with a well-known relationship between the N+ polysilicon the gate electrode and the N-well.

In a buried channel E-type PMOS, when the threshold voltage is set to about -0.5 V for low voltage operation, the sub-threshold characteristics deteriorate and the leak current increases. As a result, consumption current of the semiconductor device increases dramatically. Thus, it is difficult to use the semiconductor device in a portable apparatus such as a portable telephone.

In order to overcome the above-described problem and achieve low voltage operation and low consumption current, a

homopolar gate technique is generally used. In this technique, the conductivity type of an NMOS gate electrode is set as N-type and the conductivity type of a PMOS gate electrode is set as P-type. In this case, both the E-type NMOS and the E-type PMOS are surface channel MOS transistors. Consequently, lowering of the threshold voltage does not lead to the deterioration in sub-threshold characteristics.

However, the manufacture of a homopolar gate CMOS increases the number of processing steps and the manufacturing cost as compared with a CMOS in which the gate electrode is an N+ polycrystalline silicon monopole, since the gate polarities are separately formed for the NMOS and PMOS devices.

A reference voltage circuit is an important component of a power management semiconductor device such as a voltage detector or a regulator. A reference voltage circuit is typically comprised of an E-type NMOS and a depletion type NMOS (D-type NMOS) connected in series in many cases. When the polarity of the gate electrode is N-type, the E-type NMOS is a surface channel device while the D-NMOS is a buried channel device. An important characteristic of the reference voltage circuit is that there is a small change in output voltage with respect to a change in temperature. However, the threshold voltage of the MOS and the degree of mutual conductance relative to temperature change are very different

in surface channel and buried channel devices. As a result, the reference voltage circuit has a problem in that it is difficult to reduce the change in output voltage relative to temperature change.

The present invention provides a structure of a power management semiconductor device or an analog semiconductor device in which the goals of low cost, short manufacturing time, low voltage operation and low power consumption can be achieved.

In accordance with amended independent claim 1, the inventive CMOS semiconductor device for a voltage regulator comprises a semiconductor substrate, an N-channel MOS transistor formed in the semiconductor substrate and used in a reference voltage generating circuit of the voltage regulator, a P-channel MOS transistor formed in the semiconductor substrate and used as an output element of the voltage regulator, and a resistor formed in the semiconductor substrate, wherein a conductivity type of the gate electrodes of the N-channel MOS transistor and the P-channel MOS transistor is P-type.

In the embodiment illustrated in Fig. 1 of the drawings, the CMOS device is comprised of an NMOS 113, a PMOS 112, a P-type resistor 114 and an N-type resistor 114, all of which are formed in a P-type substrate 101. The gate

electrodes of the NMOS 113 and the PMOS 112 are formed of P+ polycrystlline silicon 107 and the source and drain regions have a single-drain structure. The PMOS 112 is formed in an N-well region 102. The resistors 114 and 115 are used for a voltage dividing circuit or a time constant circuit.

Since the gate electrode of the PMOS 112 is formed of P+ polycrystalline silicon, the E-type PMOS is a surface channel device. Thus, the setting of a threshold voltage to a level in the range of -0.5V does not lead to deterioration of the sub-threshold characteristics. Accordingly, low voltage operation and low power consumption are possible.

The E-type NMOS 113 has a buried channel. However, since arsenic can be used as a donor impurity for threshold control, the channel is an extremely shallow buried channel. Thus, any deterioration in sub-threshold characteristics and increase in leak current are greatly reduced in comparison with an E-type PMOS having a gate electrode formed of N+ polycrystalline silicon and a deep buried channel resulting from the use of boron as an acceptor impurity.

A voltage regulator employing the inventive CMOS device is shown in Fig. 3 of the application drawings. The voltage regulator has a reference voltage generating circuit 150 which uses the NMOS of the inventive circuit, an error

amplifier 151, a PMOS output element 152 and a voltage dividing circuit 157 comprised of resistances 156.

Since the size of the output element 152 largely dictates the size of the voltage regulator, the present invention serves to facilitate production of a small-sized voltage regulator because the PMOS transistor of the inventive CMOS circuit is substantially reduced in size by virtue of the P-type gate electrode.

In accordance with the present invention, a CMOS semiconductor device for a voltage regulator has an NMOS transistor used in a reference voltage generating circuit of the voltage regulator, a PMOS transistor used as an output device of the voltage regulator, and a resistor, wherein the NMOS and PMOS transistors have P-type gate electrodes.

No corresponding structure is disclosed or suggested by the prior art of record.

The CMOS circuit of Erdeljac et al. includes an NMOS transistor 44, a PMOS transistor 50 and a resistor. However, the NMOS and PMOS transistors have opposite conductivity type gate electrodes.

Figs. 59 and 60 of Yoh et al. disclose an NMOS transistor Q4 having a P-type gate electrode and a PMOS transistor Q1 with a P-type gate electrode.

However, neither Erdeljac et al. nor Yoh et al. disclose or suggest that the NMOS transistor is used in a reference voltage generating circuit of a voltage regulator and that the PMOS transistor is used as an output device of the voltage regulator.

Thus the combined teachings of the cited references fail to teach the subject matter recited by amended independent claim 1.

Nor do either of the cited references suggest the desirability of the claimed invention.

As pointed out above, a homopolar gate CMOS has gate polarities that are separately formed for the NMOS and PMOS devices. Thus, the homopolar device requires a larger number of processing steps and is more expensive than a CMOS device in which the gate electrode is an N+ polycrystalline silicon monopole.

The present invention uses the NMOS and PMOS transistors of a CMOS device in a novel and unique manner in order to take advantage of the benefits of each device. For example, the NMOS is an E-type MOS having a shallow buried channel formed using arsenic as a donor impurity. Since the channel is extremely shallow, only slight deterioration in sub-threshold characteristics and increase in leak current occur.

Since the gate electrode of the PMOS is formed of P type polycrystalline silicon, an E-type PMOS according to the present invention is a surface channel device. Thus, the setting of a threshold voltage to a level in the range of -0.5V does not lead to deterioration of the sub-threshold characteristics. Accordingly, low voltage operation and low power consumption are possible.

Accordingly, a voltage regulator employing the inventive CMOS device using the NMOS as part of the reference voltage generating circuit and the PMOS as an output device does not suffer from the drawbacks associated with the conventional device described above.

When considered as a whole, neither of the cited references would have suggested the desirability of modifying a voltage regulator circuit to use an NMOS transistor of a CMOS device in a reference voltage generating circuit of the voltage regulator and to use a PMOS transistor as an output device of the voltage regulator.

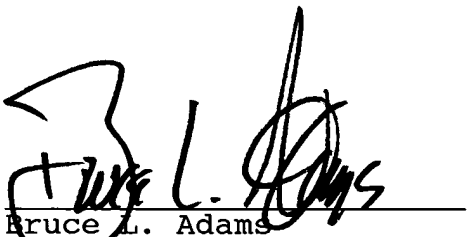
Accordingly, applicants respectfully submit that amended claim 1 patentably distinguishes over the prior art of record and that the rejections under 35 U.S.C. §103(a) should be withdrawn.

In view of the foregoing amendments and discussion, the application is believed to be in condition for allowance.

Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

ADAMS & WILKS
Attorneys for Applicants

By: 
Bruce L. Adams
Reg. No. 25,386

50 Broadway - 31st Floor
New York, NY 10004
(212) 809-3700

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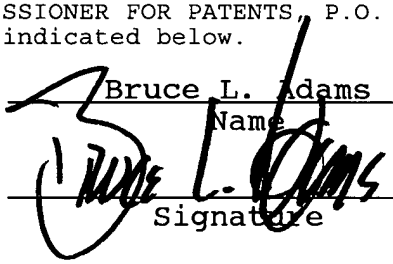
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Paragraph beginning at line 12 of page 1 has been amended as follows:

Fig. 89 is a schematic cross sectional view of a conventional semiconductor device. The semiconductor device is composed of [an] a complementary MOS structure (hereinafter referred to as NMOS) in which a gate electrode formed on a P-type semiconductor substrate is comprised of N+ type polycrystalline silicon and a P-channel MOS transistor 212 (hereinafter referred to as PMOS) in which a gate electrode formed in an N-well region is also comprised of N+type polycrystalline silicon, and a resistor 215 used in a voltage dividing circuit for dividing a voltage which is formed on a field insulating film or a CR circuit for setting a time constant. The resistor is formed of a polycrystalline silicon that is the same layer as a gate electrode of CMOS with N-type conductivity and has the same conductivity type in terms of simplicity and [easiness] ease of a method of manufacturing thereof.

Paragraph beginning at line 20 of page 2 has be n amended as follows:

In the buried channel E-type PMOS, in the case where the threshold voltage is set to, for example, -0.5 V or more for low voltage operation, a sub-threshold characteristic, which is one index of low voltage operation of a MOS transistor, extremely deteriorates, and thus, a leak current at the off time [of off of] the PMOS increases. As a result, consumption current at the time of waiting of the semiconductor device remarkably increases. Thus, there is problem in that it is difficult to apply the semiconductor device to portable apparatuses typified by a portable telephone and a portable terminal which re greatly demanded in recent years and [of which] the market for which is predicted [that it will] to further develop in the future.

Paragraph beginning at line 5 of page 95 has been amended as follows:

P+polycrystalline silicon that is a source and a gate of the D-type NMOS 126 is short-circuited by a wiring metal though not shown in the figure, and further, the drain is connected with a high voltage supply terminal 123 showing the D-type NMOS 126.

IN THE CLAIMS:

Claims 1, 2, 4, 11, 15, 16, 43 and 54 have been amended as follows:

1. (Amended) A complementary MOS semiconductor device for a voltage regulator, comprising: a semiconductor substrate; [having] an N-channel MOS transistor formed in the semiconductor substrate and used in a reference voltage generating circuit of the voltage regulator; [,] a P-channel MOS transistor formed in the semiconductor substrate and used as an output element of the voltage regulator; and a resistor[,] formed in the semiconductor substrate; wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type.

2. (Amended) A complementary MOS semiconductor device according to claim 1;[,] wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each comprise a single layer of [first] polycrystalline silicon having a film thickness in a range of 2000 Å to 6000 Å and including boron or BF_2 with an impurity concentration of at least 1×10^{19} atoms/cm^3 [or more].

4. (Amended) A complementary MOS semiconductor device according to of claim 1;[,] wherein the resistor is a polycrystalline silicon resistor formed in the same layer and [has] having the same film thickness range as the [first] polycrystalline silicon constituting the gate [electrode] electrodes of the N-type transistor and the P-type transistor.

11. (Amended) A complementary MOS semiconductor device according to claim 1; [,] wherein the N-channel MOS transistor and the P-channel MOS transistor have [include a MOS transistor having] a [first structure of a] single drain structure comprising a diffusion layer with a high impurity concentration, and [in which] a source and a drain of the N-channel MOS transistor and the P-channel MOS transistor overlap the P-type gate electrode in a planar manner.

15. (Amended) A complementary MOS semiconductor device according to claim 1; [,] wherein [, in] the N-channel MOS transistor[,] has a buried channel and [in which] a threshold voltage [is] in an enhancement mode [is a buried channel].

16. (Amended) A complementary MOS semiconductor device according to claim 1;[,] wherein [, in] the P-channel MOS transistor[,] has a surface channel and [in which] a

threshold voltage [is] in an enhancement mode [is a surface channel].

43. (Amended) A complementary MOS semiconductor device according to claim 1; [,] wherein the semiconductor substrate is a P-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are [defined by forming] formed in an N-type well in the semiconductor substrate[, respectively].

54. (Amended) A complementary MOS semiconductor device according to claim 1;[, ,] wherein the [first] polycrystalline silicon is formed by [a] chemical vapor deposition [method].